REMARKS

In response to the Examiner's Action mailed on Nov. 1, 2004, claims 1 to 60 are amended. The applicant hereby respectfully requests that the patent application be reconsidered.

An item-by-item response to Examiner's objections or rejections is provided in the followings:

1. *Rejection of Claims under 35 USC §102*

The Examiner rejects claims 1 to 51 under 35 U.S.C.102(e) as being anticipated by Patel et al. (US 2004/0125347). According to the Examiner, claim 1, Patel et a1 discloses, in figures 2 and 3A, an electromechanical micromirror device (200), comprising: a device substrate (202) with a 1st surface and a 2nd surface; control circuitry (not shown, figure 2 shows the 2"~ surface of the device substrate) disposed on said 1st surface of said substrate, and a micro-mirror section *(215)* disposed on said 2nd surface of said substrate, wherein said micromirror section (215) comprises: a micromirror (201), and at least I support structure (230) for supporting said micromirror (201) (sections 0047 and 0048). For claim 2, Patel et al. discloses, in figures 2 and 3A, an electromechanical micromirror device (200), wherein said control circuitry is selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DM05 circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, hiP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits (section 0043). Furthermore, according to the Examiner, in other figures and descriptions of Patel et al., other elements included in claims 3 to 51 are also disclosed. For these reasons, the Examiner rejects claims 1 to 51 on

the basis that Patel et al. anticipate the inventions as that directed by claims 1 to 51.

In response to the rejections, claims 1 to 51 are amended. The amended claims are directed to invention that the micromirrors and the circuitry are formed and supported on a single substrate. Specifically, in the amended claim 1, the invention is directed to an electromechanical micromirror device, comprising:

a) a **single** substrate with a 1st surface and a 2nd surface;
b) a control circuitry disposed on said 1st surface of said **single** substrate; and
c) a micromirror section disposed on said 2nd surface of said single substrate wherein said micromirror section comprises:
    i) a micromirror; and
    ii) at least one support structure for supporting said micromirror.

Claim 17 is also amended to directed to an array of electromechanical micromirror devices comprising:

a) a **single** substrate with a 1st surface and a 2nd surface;
b) a control circuitry disposed on said 1st surface of said substrate; and
c) an array of micromirror sections disposed on said 2nd surface of said single substrate wherein each said micromirror section comprises a micromirror; and
d) a support structure for supporting said micromirror.

Claim 34 is also amended to direct to a method of fabricating an array of electromechanical micromirrors comprising the steps of:

a) providing a single substrate with a 1st surface and a 2nd surface;
b) forming control circuitry on said 1st surface of said single substrate; and

c) forming a plurality of support structures on said second surface of said single substrate and forming a plurality of micromirrors on top of and supported by said support structures.

The amended claims 1 to 51 are therefore totally different and novel over Patel etl al. Specifically, Patel et al. discloses a method and structure for manufacturing micromirrors that employ two substrates, e.g., a glass substrate 280 and a silicon wafer 281 in Figs. 4A to 5A in Patel et al. The amended claims 1 to 51 are therefore different, novel and not obvious over Patel et al.

2. *Rejection of Claims under 35 USC §103*

The Examiner rejects claims 52-60 under 35 U.S.C.103(a) as being unpatentable over Patel et al. in view of Chiu et al. (US 6,639,713). According to the Examiner, for claim 52, Patel et al. disclose a method of fabricating an array of electromechanical micromirror devices, comprising the steps of forming control circuitry (not shown, figure 2 shows the 2 surface of the device substrate); forming a plurality of micromirror sections (215) on said exposed insulator layer, comprising the steps of forming a plurality of support structures (230) for supporting micromirrors (201), and forming a plurality of micromirrors (201) such that each said micromirror (201) is supported by at least 1 said support structure (230) (sections 0047 and 0048) except that it does not show providing a silicon-on-insulator substrate with an epitaxial top silicon layer, an insulator layer, and a bottom silicon layer forming control circuitry on said epitaxial top silicon layer, removing said bottom silicon layer, thereby exposing the insulator layer. Chiu et al. shows that it is known to provide a silicon-on-insulator substrate with an epitaxial top silicon layer (321), an insulator layer (323), and a bottom silicon layer (324) on said epitaxial top silicon layer, removing said bottom silicon layer, thereby exposing the insulator layer for at least partially intercepting a

light beam propagating along a beam path (col. 15, lines 51-53 and col. 21, lines 37-52). Therefore it would have been obvious to someone of ordinary skill in the art at the time the invention was made to combine the device of Patel et al. with the silicon-on-insulator substrate of Chiu et al. for the purpose of at least partially intercepting a light beam propagating along a beam path (col. 15, lines 5 1-53 and col. 21, lines 3 7-52). Regarding claim 53, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of forming control circuitry comprises a step of fabricating circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, and DMOS circuits (section 0043). Regarding claim 54, Patel et al. discloses a method of fabricating an array of electromechanical micromirror devices, including a step of removing said bottom silicon layer but does not specifically disclose removing the bottom silicon layer by back-grinding. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the process of back-grinding for the purpose of ensuring the eradication of the silicon layer on the substrate. Regarding claim 55, Patel et al. discloses, in figures 6A-6H, a method of fabricating an array of electromechanical micromirror devices, wherein said step of removing said bottom silicon layer comprises chemical mechanical polishing (CMP) (section 0062). The Examiner further rejects claims 54 to 60 on the bases of the inventions disclosed by Patel et al. in view of Chiu et al. According to the Examiner, Patel et al. and Chiu et al. combined would have made the inventions directed by claims 52-60 obvious.

In response to the rejections, claims 52 to 60 are amended. The amended claim 52 is directed to a method of fabricating an array of electromechanical micromirrors, comprising the steps of:

a) providing a **single** silicon-on-insulator substrate with an epitaxial top silicon layer above an insulator layer, ~~supported by~~ a bottom silicon layer;

b) forming control circuitry on said epitaxial top silicon layer;
c) removing said bottom silicon layer, thereby exposing the insulator layer;
d) forming a plurality of support structures followed by forming a plurality of micromirrors on top of and supported by said support structures.

The amended claims 52 to 60 are totally different and not obvious over Patel and Chiu. The device and the method of manufacturing optical devices disclosed by Patel and Chiu are based on two substrates. The method of manufacturing an array of electromechanical micromirrors as now directed by the amended claims 52 to 60 are supported and fabricated on a single substrate. The method and the structures are different, novel and non-obvious over Patel et al. in view of Chiu et al.

With the amended claims and the reasons provided above, the applicant hereby respectfully requests that Examiner's rejections under 35 USC § 102 and 35 USC § 103 be withdrawn and the present application be allowed.

Respectfully submitted
Fusao Ishii

By 

Bo-In Lin - Attorney, Registration No. 33,948
13445 Mandoli Drive, Los Altos Hills, CA 94022
(650) 949-0418 (Tel), (650) 949-4118 (Fax)

January 26, 2005